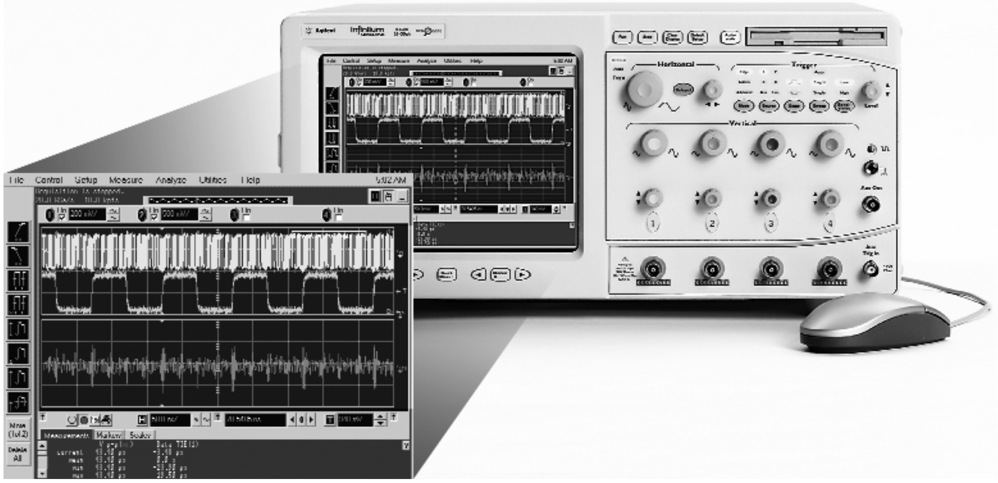
Memory-Depth Requirements for Serial Data Analysis in a Real-Time Oscilloscope

Application Note 1495



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Introduction

If you are designing high-speed devices that employ embedded clocks, you need to be able to characterize serial data streams. You can use Agilent Technologies' 54830 and 54850 Series Infiniium real-time oscilloscopes along with Agilent E2688A high-speed serial data analysis (SDA) software for this task. Before you begin, however, you need to ensure that your oscilloscope has enough memory for serial data and jitter analysis. How much memory you need depends on what you were trying to accomplish. This application note examines some common validation and troubleshooting tasks to determine how much memory you need. We will look at memory requirements for:

- Examining low-frequency or infrequently occurring jitter
- Examining all the combinations of bit sequences in a pseudorandom binary sequence (PRBS)
- Achieving a desired confidence level of meeting a bit-error-rate goal

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Low-frequency, or infrequently occurring jitter

If the serial data signal is modulated at a low frequency, and you want to measure the jitter, you need a certain minimum memory depth. For example, if you have a 2.5 Gb/s signal captured by a scope with a 20 GSa/s sampling rate and 1 M of memory, you capture 50 microseconds of elapsed time, which would allow you to view one cycle of jitter at a frequency of 20 kHz.

Measuring low-frequency jitter is sometimes not important, as the clock recovery phase-locked loop (PLL) in most serial data receivers can reject jitter at low frequencies. But sometimes an event occurring at a low repetition rate can cause bursts of jitter or noise that contain higher frequencies that the PLL cannot reject. An example is shown in Figure 1. The top (yellow) trace is a serial data signal. The middle (green) trace is an uncorrelated aggressor signal that is inducing short-term bursts of jitter in the data signal. The bottom (purple) trace is a jitter trend signal, which is simply a time plot of the timing of each edge in the data stream compared to the "ideal" recovered clock. You can see that there is a burst of timing errors that coincides with each transition in the green aggressor signal.

If the data rate of your signal allows it, you may be able to use a lower sampling rate to extend the time duration captured on each trigger. For example, for a data rate of 1 Gb/s and a rise time of 300 ps, you would be able to capture all the frequency content of the signal sufficiently at a sampling rate of 10 Gb/s. In this case, 1 M of memory would capture 100 microseconds worth of data, allowing you to see a full cycle of jitter at 10 kHz.

Table 1 shows the minimum jitter frequency, or burst occurrence rate, that can be captured as a function of memory depth, for a sampling rate of 20 GSa/s.

Tip: If you suspect something in your power supply is sending out bursts of noise or jitter at power line crossovers, you can trigger on the power line and see if there is a stable burst on the jitter trend waveform. If you do see a stable burst, it confirms your hypothesis.

Most switching power supplies operate above 20 kHz, so 1 M memory in a scope sampling at 20 GSa/s is usually sufficient to capture problems that are correlated to switching power supplies.

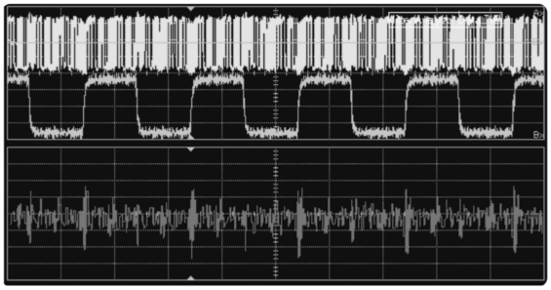

Figure 1. Jitter on a signal (top, yellow trace) caused by coupling from another signal (middle, green trace).

Memory depth, samples	Time duration of capture (seconds)	Lowest frequency captured (one full cycle)
256 K	1.28E-5	78.13 kHz
1 M	5E-5	20 kHz
32 M	1.6E-3	625 Hz
100 M	5E-3	200 Hz

Table 1. Memory depth, time duration of capture, and lowest frequency captured, for a sampling rate of 20 GSa/s.

Examining all the combinations in a pseudorandom binary sequence

The advantage of using a pseudorandom binary sequence as a stimulus in testing systems is that it contains all the possible sequences of numbers of ones and zeros, limited only by the length of the PRBS. A 2^N-1 PRBS sequence will contain one sequence of N-1 zeros followed by N ones, along with all combinations of <N zeros followed by <N ones.

The length of PRBS pattern you should use depends on the serial bus that you are designing. The longest run of consecutive ones or zeros in the PRBS you choose should match the longest consecutive run of ones or zeros in the serial bus you're designing. If your bus uses 8b/10b encoding, for example, you only need to test using a 2^5-1 PRBS.

To view the effects of all the various combinations, you should capture the entire PRBS. If you analyze a single acquisition that is shorter than the entire PRBS, you will be missing some combinations. By running repetitively, you may still have a fair chance of seeing all parts of the sequence after some indeterminate time, as the scope will most likely retrigger more or less randomly at various points within the PRBS. But capturing the entire PRBS on each trigger gives you 100 percent assurance.

Table 2 shows the memory required to capture all of a PRBS sequence for a 2.5 Gb/s bit rate and a scope sampling at 20 GSa/s. The math is very straightforward for other combinations:

Number of cycles captured =
[(memory depth) x (data rate)]/
(scope sampling rate)

2^7-1 and 2^{11}-1 are commonly used pattern durations; both fit easily in 256 K of memory. A 2^{16}-1 sequence will fit in 1 M of memory. For sequence lengths not shown in Table 2, or for other sampling rates and data rates, you can easily calculate the memory required.

PRBS length	Unit intervals in entire sequence	Memory required (samples)
2^7-1	127	1 K
2^{11}-1	2047	16 K
2^{16}-1	6.554E4	524 K
2^{32}-1	4.29E9	3.44E10

Table 2. Memory required to capture various PRBS lengths, for a bit rate of 2.5 Gb/s and a sampling rate of 20 GSa/s.

Extrapolating to a desired bit error rate

How long do you need to let a scope mask or jitter test run before you can feel confident your system will meet a given bit error rate (BER)?

For a bit error rate of, say, 10^{-12}, you could have a large number of errors in the first few bits you examine; on the other hand, you also could see zero errors in 10^{16} (or any arbitrarily large number) of consecutive bits. You could determine the bit error rate with near 100 percent confidence, but this could take an unnecessarily long time, especially if you never see any violations. Assuming you get no violations, you can calculate the confidence interval for predicting a given error rate from less data. Table 3 shows how many error-free bits you would have to observe to achieve the indicated confidence level for a given BER.

Although the correlation between a scope and a bit error ratio tester (BERT) is quite good, a scope gives you an estimate of the bit error rate, not a measurement. To achieve the ultimate confidence that you've met your error rate goals, you'll need to use a BERT. This is particularly true for very small error rates. The problem is that the scope's jitter noise floor and vertical noise floor begin to creep into the measurement and set a floor on the measurable error rate.

If you do see some errors, then the numbers in Table 3 are invalid and you cannot extrapolate from them. In that case, you need to let the system run until you see 10-15 errors to have good confidence that the number of violations divided by the number of unit intervals (UIs) tested is a good predictor of the long-term bit error rate. That can take an indeterminate length of time, assuming errors occur randomly.

Table 4 shows the relationship between memory depth, number of UIs captured on each acquisition, and the total number of acquisitions required to achieve 95 percent and 99 percent confidence of $<10^{-12}$ BER. The table assumes, again, a 2.5 Gb/s data rate and a scope sampling at 20 GSa/s.

The E2688A serial data analysis packages will report the number of UIs examined and the number of failed UIs. You can calculate how many unit intervals are contained in each acquisition:

Number of UIs =
(memory time duration) x (bit rate)

Memory time duration =
(memory depth)/(sampling rate)

Thus (number of UIs) =
[(memory depth) x (bit rate)]/
(sampling rate)

Confidence level	Number of unit intervals without violation required
95%	3.84/BER
99%	6.66/BER

Table 3. Confidence level as a function of number of unit intervals.

Memory depth	UIs captured at bit rate = 2.5 Gb/s, sampling rate = 20 GSa/s	Number of violation-free acquisitions to achieve 95% confidence of BER $<10^{-12}$	Number of violation-free acquisitions to achieve 99% confidence of BER $<10^{-12}$
256 K	32 K	1.2E8	2.881E8
1 M	125 K	3.072E7	5.328E7
32 M	4 M	9.6E5	1.665E6
100 M	12.5 M	3.072E5	5.328E5

Table 4. Memory depth and number of violation-free acquisitions needed to achieve 95% and 99% confidence in 10^{-12} BER, with a bit rate of 2.5 Gb/s and a sampling rate of 20 GSa/s.

Advantages of software clock recovery

If statistical confidence is important, it’s worth mentioning that scopes that recover the clock in software and reconstruct the eye from that clock have significant advantages over older methods of eye diagram measurements. In the days of separate clock and data signals, you triggered the scope on the clock signal and viewed an eye diagram of the data signal. This led to the following limitations:

Trigger jitter

Trigger jitter in the scope added to the jitter of the measurement. With software clock recovery, trigger jitter does not affect the measurement results at all. The scope could be triggered on anything, or free-running with no active trigger source at all.

False trigger

All scopes have some rate of false triggers, caused by violation of setup and hold in the trigger flip-flops. While the rate of false triggers is very low, it can affect the measurement statistics for very low bit-error rates. Once again, with software clock recovery, false triggers are not a problem.

Conclusion

The scope memory depth required to analyze serial data signals depends on the task you intend to accomplish. The guidelines in this application note should help you decide how much memory you need.

Glossary

Bit error ratio The number of bits with errors divided by the total number of bits that have been transmitted, received or processed over a given time period

Jitter Timing error associated with the placement of digital signal edge transitions relative to their ideal location. This timing error, often referred to as time interval error (TIE) or phase jitter, can be composed of both deterministic and random error sources.

Real-time oscilloscope An oscilloscope that uses high-speed sampling in order to capture signals in a single-shot acquisition

8b/10b encoding A method of encoding serial data to ensure a sufficient frequency of transitions to maintain synchronization of the clock and data recovery phase-locked loop. 10 bits are transmitted for every 8 bits of data.

Related Literature

Publication Title	Publication Type	Publication Number
Infiniium 54830 Series Oscilloscopes	Data Sheet	5988-3788EN
Infiniium 54850 Series Oscilloscopes *InfiniiMax 1130 Series Probes*	Data Sheet	5988-7976EN
Agilent Technologies E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium 54830 and 54850 Series Oscilloscopes	Data Sheet	5989-0108EN

Product Web site

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